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1.0 GENERAL

1.1 GENERAL DESCRIPTION

The Computer Monitor Adapter (CMA) will be an IOM channel in the DATANET 355 intended for use in message switching systems to perform the following functions:

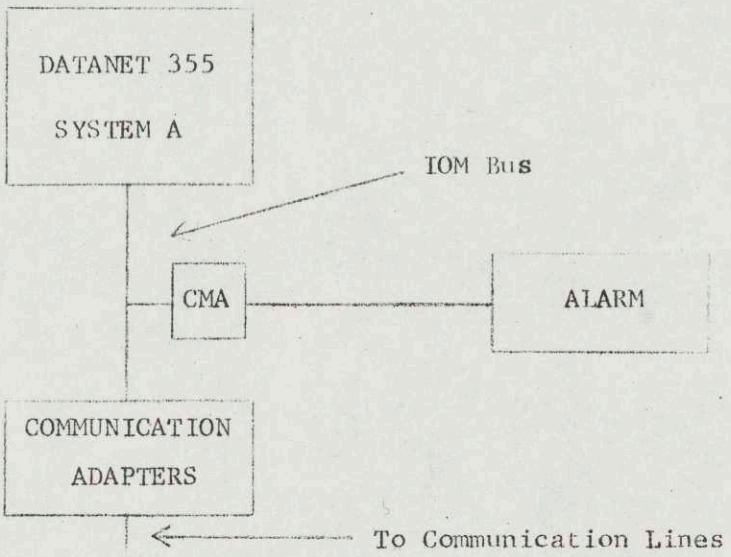
- o System confidence monitoring (single or dual systems)
- o Inter-system data communication (dual systems only)
- o Communication line switch control (dual systems only)

The connection of the CMA in single and dual system configurations is illustrated in Figure 1.

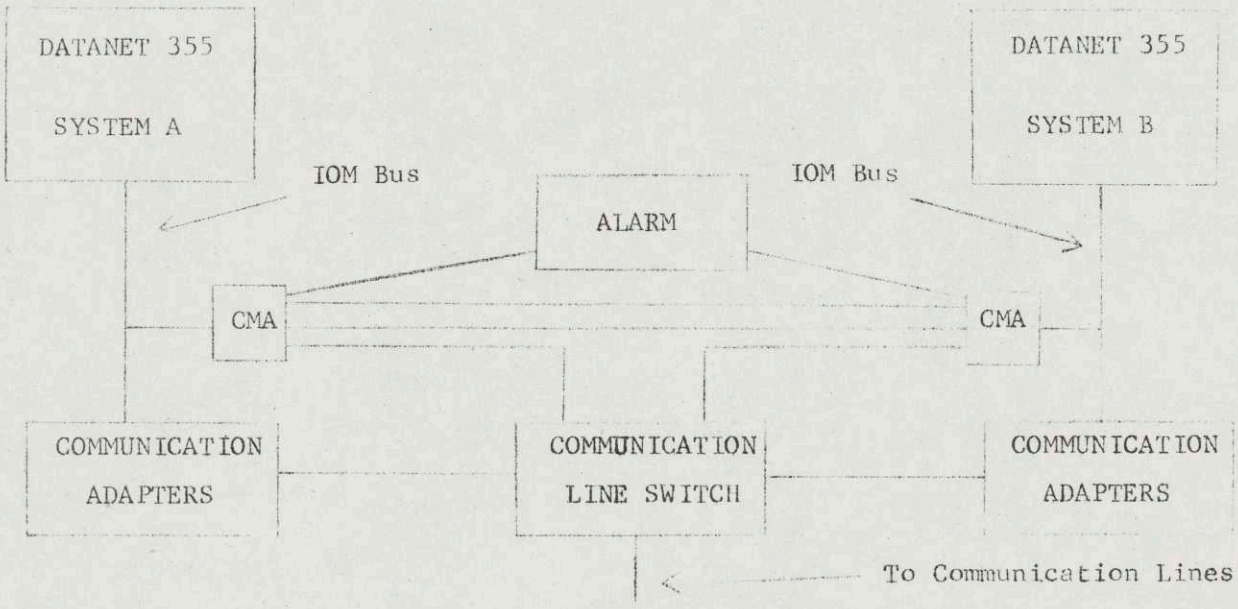
In single-system configurations the CMA will monitor the system's operational status by means of a hardware "dead-man" timer which must be reset periodically by the 355 program. If the timer should run out before being reset, a System Confidence signal, generated by the CMA, will be turned off. This signal will be used to activate an external alarm in order to alert the operator.

In dual-system message switching configurations a CMA will monitor each system's operational status as described above, but, in addition to activating an external alarm, the System Confidence signal will be used to signal the other system and the communication line switch so that system recovery may be effected.

The CMA will also provide for data communication between the systems in a dual configuration so that the on-line system may periodically update the communication tables as required for system recovery.



Single-System Message Switching Configuration



Dual-System Message Switching Configuration

FIGURE 1 - CMA INTERCONNECTION IN SINGLE- AND DUAL-SYSTEM CONFIGURATIONS

1.2 PHYSICAL DESCRIPTION

The CMA channel will be contained on a single MQX-type integrated circuit board which will be mounted in one of the slots which interface with the DATANET 355 IOM bus.

All interface signals between the IOM and the CMA will be via the backpanel-wired IOM bus. Connections between the CMA and external devices (other system CMA, communication line switch and external alarm) will be via free-edge connectors on the CMA.

1.3 REFERENCE DOCUMENTS

The following documents apply toward a complete specification of the Computer Monitor Adapter:

Engineering Product Specification, Part 1, 355 Computer, 43A219608.

Engineering Product Specification, Part 1, DATANET 355, 43A219609.

Message Switching System, 43A239717.

Communication Line Switch EPS-1 (to be supplied).

Engineering Product Specification, Part 1, General Design Requirements for the 655 and 355 Systems, 43A177851.

Engineering Product Specification, Part 1, 355 Computer Maintainability Design, 43A177873.

2.0 FUNCTIONAL CAPABILITIES

2.1 GENERAL CAPABILITIES

The CMA will be capable of two-way-simultaneous data communication with the CMA in the other system of a dual configuration at rates up to 64,000 9-bit bytes per second. Data transmission and reception will proceed independently of program control once initiated by the program. Transmission of data between the CMA and the IOM and between CMA's in a dual system configuration will be protected by byte parity. The data transfer operation is described in Section 3.4.

By means of the System Confidence signal and a programmable Switch Control signal, the CMA will be capable of causing switch-over to a standby system in dual configurations either automatically, in the case of a system failure, or when initiated by an operator or T&D program.

2.2 PRODUCT OPTIONS

The external alarm provided with the CMA will be a visual alarm. A product option which should be initially available on the CMA is an audible alarm, which, when installed, will be activated simultaneously with the visual alarm.

2.3 CHANNEL CONFIGURATION PATCHING

The CMA will have the following parameters determined by patch modules:

- o Channel Number
- o Program Interrupt Level (Send and Receive)
- o Indirect Control Word Base Address
- o Dead-Man Timer Duration
- o Data Response Timer Duration

The patching requirements for each of these are specified in the following sections.

2.3.1 Channel Number Patch

The CMA channel number patching will consist of a patchable six-bit field which will be switched onto the IOM bus during the channel instruction cycle (see Section 3.3). This field must be capable of being patched to any six-bit code. The channel must also be capable of recognizing (decoding) this same six-bit code.

For ease of system configuration and to insure against configuration error, it is desirable that the channel decode patch and the channel number patch be the same physical patch.

2.3.2 Program Interrupt Level Patch

The CMA has two distinct interrupt conditions for which it must provide two different program interrupt levels. These interrupts are Send and Receive.

The 355 IOM interface has provisions for 16 program interrupt levels per channel. The CMA must be capable of directing either of the two interrupt conditions into any of the 16 levels by patching.

2.3.3 Indirect Control Word Base Address Patch

The Indirect Control Word (ICW) base address shall be patched within the range of 460_8 to 770_8, modulo 8. The locations of the channel ICW's with respect to the ICW base address will be as follows:

- The ICW Base Address will be the location of the Receive ICW
- The ICW Base Address + 2 will be the location of the Send ICW
- The ICW Base Address + 4 will be the location of the Send Status ICW
- The ICW Base Address + 6 will be the location of the Receive Status ICW.

2.3.4 Dead-Man Timer Duration Patch

The duration of the dead-man timer, used for monitoring the system's operational status, will be determined by the channel configuration patching. The nominal time durations selectable by pathing will be 250 milliseconds, 500 milliseconds and 1 second. Discussion of this timer in this document (see Section 3.6) will assume the 1 second duration.

2.3.5 Data Response Timer Duration Patch

The duration of the data response timer, used in transferring a byte of data from one system to another, will be determined by the channel configuration patching. Nominal time durations selectable by patching will be 125 milliseconds and 250 milliseconds. Discussion of this timer in this document (see Sections 3.4.1 and 3.4.2) will assume the 250 millisecond duration.

3.0 OPERATION

3.1 GENERAL OPERATION

Operation of the CMA will be under control of the 355 program which will generate Peripheral Control Words (PCW's) containing commands for the CMA and will send them to the CMA via the IOM using the SEL and CIOC instructions.

When activated by the program, the CMA will issue channel instructions to the IOM to request service as required for data transfer and status storage. When data transfer is completed or status is stored, the CMA will interrupt the 355 program.

3.2 CONTROL WORDS

The CMA will use five types of control words for control of the channel and for data transfers. These five control words are:

- One 36-bit Peripheral Control Word (PCW)
- One 36-bit Receive Indirect Control Word (ICW)
- One 36-bit Send Indirect Control Word
- One 36-bit Send Status Indirect Control Word
- One 36-bit Receive Status Indirect Control Word

The formats for these control words are defined in the following sections.

3.2.1 Peripheral Control Words (PCW's)

The general format of the PCW used for control of the CMA will be as follows:

Bit #	0 — 22	23 — 29	30 — 32	33 — 35
	Not Used - MBZ	Command	Spare MBZ	Op Code
# of Bits	23	7	3	3

The 7 command bits in the PCW will be used for sending broadside commands to the CMA and will be encoded as follows:

Bit #	Function
23	Mask Channel
24	Timer Control
25	Receive Mode
26	Send Mode
27	Wraparound Mode
28	Switch Control
29	Parity Test

The 3 Op Code bits will be encoded (bit 33 = MSB) as follows:

Op Code	Function
0_8	(no op)
1_8	Timer reset
2_8	Request Send Status
3_8	Request Receive Status
4_8 to 7_8	(spare)

3.2.1 Peripheral Control Words (continued)

When a PCW is sent to the CMA, the command bits will cause the following actions by the CMA.

Bit #	Action by CMA
23	When a 1, the channel is masked and initialized and will not request service of the IOM; when a 0, the channel is unmasked and may request IOM service as necessary for normal operation.
24	When a 1, the CMA "dead-man" timer will be enabled; when a 0, the timer will be stopped.
25	When a 1, the CMA receive mode logic will be enabled; when a 0, it will be disabled.
26	When a 1, the CMA send mode logic will be enabled; when a 0, it will be disabled.
27	When a 1, the CMA external interface lines will be wrapped back on one another as detailed in Section 6.3; when a 0, the external interface lines of the CMA will be returned to their normal operational state.
28	When a 1, the Switch Control lead to the associated Communication Line Switch will be turned on (indicating the systems "permission" to be placed on-line); when a 0, the Switch Control lead will be turned off.
29	When a 1, the CMA send logic will be forced to generate wrong parity (even) on data bytes to be sent while in the wraparound mode. When a 0, normal odd parity will be generated. This bit will be interpreted by the CMA only when in the wraparound mode (PCW bit 27 = 1). See Section 6.3.

3.2.1 Peripheral Control Words (continued)

The Op Codes contained in a PCW sent to the CMA will cause the following actions by the CMA.

Op Code	Action by CMA
0	No action caused by this Op Code. Used in conjunction with broadside commands not requiring any Op Code.
1	Causes the "dead-man" timer to be reset to the beginning of its timing cycle. This Op Code will be ignored if sent when the timer is disabled by the action of command bit 24.
2	Causes the CMA to store its Send Status and cause a Send Status Interrupt.
3	Causes the CMA to store its Receive Status and cause a Receive Status Interrupt.
4-7	(spare - reserved for future use)

3.2.2 Indirect Control Words (ICW's)

Indirect data transfers between the CMA and the 355 core storage will be effected by the IOM through the use of ICW's - one for send data, one for receive data, one for send status and one for receive status. The ICW's will be stored in the 355 core storage in locations based on the ICW Base Address as explained in Section 2.3.3.

The core storage address of the appropriate ICW will be presented to the IOM by the CMA when an indirect data transfer is requested by the CMA.

All four ICW's will have the same format as follows:

Bit #	0 2	3 17	18 22	23	24 35
	C	Address	MBZ	E	Character Tally
# of Bits	3	15	5	1	12

The functions of the ICW fields are detailed in EPS-1 for the 355 Computer. The C-field (character size) should contain 010 or 011 (9-bit characters) for the Send ICW and the Receive ICW and 000 (18-bit word) for Send Status and Receive Status ICW's.

3.3 CHANNEL INSTRUCTIONS

Channel instructions will be generated by the CMA to request specific operations by the IOM. These instructions will be presented to the IOM on the command bus as detailed in the 355 Computer EPS-1. Only two operation codes and two set interrupt cell operation code will be generated by the CMA. These are:

Op codes:	LCM (load channel from storage)
	SCM (store channel in storage)
Interrupt codes:	NSX (no interrupt cycle)
	SXC (set interrupt cell unconditionally)

As explained in Section 2.3.2 the interrupt level appearing on the command bus during the instruction cycle will be patchable to any of the 16 possible levels. The particular type of interrupt being set will be determined by this level.

3.4 DATA TRANSFER

The exchange of data between the two systems of a dual 355 configuration will be accomplished through the CMA's in the two systems. The exchange will be initiated by the program in the 355 that is sending the data and, once started, will normally proceed independently of either 355's program until the exchange is completed. Transmission and reception of data will be accomplished as explained in the following sections.

3.4.1 Data Transmission

Transmission of data to the other system in a dual configuration will be initiated by the 355 program. The program must first set up a transmit buffer area and associated send ICW and then issue a PCW to the CMA to set the send mode. This will cause the channel to give a "send mode on" indication to the other system CMA and start a 250 millisecond (nominal) send mode response timer. If the other system CMA does not respond within this time period with a "receive mode on" indication, the CMA will reset its send mode, store send status and cause a send status interrupt.

If the other system responds within the allotted time period with a receive mode on indication (or if the other system's receive mode was set prior to setting the send mode), the CMA will request the first send data byte (indirect load).

When the channel obtains a data byte on the 9 least significant bits of the B Bus it will check it for odd parity (compare with parity line on IOM bus), buffer it, generate odd parity for the byte and present it at the interface to the other system as a 10-bit (9 + odd parity) byte. When the data byte is available at the interface, the send logic will generate a Data Available strobe to signal the other system. The other system will, in return, answer with a Response Strobe and a Data Received signal which indicates that the data was correctly received. The CMA will continue requesting data bytes from the IOM and sending them to the other system at an average rate of up to 64,000 bytes per second until the last data byte has been sent.

When the last byte is obtained from the IOM, it will be accompanied by a Pre Tally Run Out (PTRO) signal. The PTRO will cause the CMA to terminate the send mode, store the channel's send status, and cause a send status interrupt of the program to notify the 355 that the transmission has been completed. The occurrence of a Tally Run Out (TRO) is an error condition and will, likewise, cause termination of the send mode, send status storage and a program interrupt.

If, during the data transmission process, an indication of a detected parity error is received from the other system, the CMA will note this status in the send status word at the completion of the transmission. Data transmission will not be interrupted when the parity error is indicated.

3.4.1 Data Transmission (continued)

If either of two abnormal situations occurs during the transmission of data to the other system, the CMA will terminate the send mode, store send status, and interrupt the 355 program. These two abnormal situations are:

1) The other system does not respond to a Data Available strobe within a nominal 250 millisecond time period.

2) The other system turns its receive mode off.

3.4.2 Data Reception

When a "send mode on" indication is received from the other system, indicating a request to transfer data, the 355 program will be interrupted (receive status interrupt). The 355 program must set up a receive buffer area and associated ICW and issue a PCW to the CMA to set the receive mode. This must all be accomplished within the nominal 250 millisecond time interval allowed by the other system CMA send mode response timer or prior to the setting of the send mode.

When the receive mode is set, the CMA will continually look for the Data Available strobe from the other system. When the strobe is received, the CMA will buffer the 10-bit byte appearing on the data lines from the other system and check the byte for correct odd parity. The received data byte will be placed on the 9 least-significant bits of the C Bus and the odd parity bit on the parity line and an indirect store will be requested of the IOM. If the parity is correct the CMA will turn its Data Received signal on and generate a Response strobe (after the completion of the indirect store cycle) to signal the other system. The CMA will continue to receive, store and acknowledge bytes until the other system turns its send mode off - signalling the end of the transmission. At this point, the CMA will terminate the receive mode, store receive status, and interrupt the 355 program to notify it that the reception of data has been completed. The program must again set the receive mode, in response to the other system's send mode indication, after setting up a new receive buffer, before a second block of data may be received.

If a parity error should be detected on a received data byte, the CMA will respond to the other system with a Response strobe with the Data Received signal remaining off. The parity error will be indicated in the receive status word stored at the end of the receive operation.

3.4.2 Data Reception (continued

If a Pre Tally Run Out (PTRO) or Tally Run Out (TRO) indication is received from the IOM when requesting an indirect store of a received data byte, the CMA will store receive status and interrupt the 355 program. The program may then issue a PCW to reset the receive mode which, in turn, will cause termination of the send mode in the other system (see Section 3.4.1).

3.5 STATUS WORDS

Two types of status will be stored by the CMA - send status and receive status. These status words will be placed on the least signficant bit positions of the C Bus (corresponding to the bit positions in an 18-bit 355 word) as indicated in Figure 2.

C Bus Bit	Send Status	Receive Status
17	Line Switch Mode (1)	Line Switch Mode
16	Line Switch Position (1)	Line Switch Position
15	System Confidence (other system) (1)	System Confidence (other system)
14	Switch Control (other system) (1)	Switch Control (other system)
13	Switch Control	Switch Control
12	Wraparound Mode	Wraparound Mode
11	Send Mode	Send Mode
10	Receive Mode	Receive Mode
9	Timer Control	Timer Control
8	Send PTRO (2)	Receive PTRO (3)
7	Send TRO (2)	Receive TRO (3)
6	Parity error on byte sent	Parity error on byte received
5	Transmission terminated by receiving system (2)	Send Mode (other system) (4)
4	Data parity error (IOM to CMA)	Data parity error (CMA to IOM)
3	PCW parity error (2)	-
2	Send mode response timeout (2)	-

Notes: (1) Causes a send status interrupt whenever change in state occurs.
(2) Causes a send status interrupt whenever bit goes to a one.
(3) Causes a receive status interrupt whenever bit goes to a one.
(4) Causes a receive status interrupt whenever change in state occurs.

FIGURE 2 - STATUS WORD FORMATS

3.5 STATUS WORDS (continued)

The functions of the send status word bits are as follows:

Bit	Function
17	When a 1, indicates that the line transfer switch is in the "automatic" mode of operation. When a 0, indicates that the line transfer switch is in the "manual" mode of operation.
16	When a 1, indicates that the system is connected to the communication lines. When a 0, indicates that the system is not connected to the communication lines (other system on-line).
15	When a 1, the System Confidence signal from the other system CMA is on. When a 0, it is off.
14	When a 1, the Switch Control signal from the other system CMA is on. When a 0, it is off.
13	When a 1, the Switch Control signal (this CMA) is on. When a 0, it is off.
12	When a 1, the CMA is in the Wraparound Mode. When a 0, it is not.
11	When a 1, the CMA's send logic is enabled. When a 0, it is not.
10	When a 1, the CMA's receive logic is enabled. When a 0, it is not.
9	When a 1, the "dead-man" timer is enabled. When a 0, it is not.
8	When a 1, a send pre tally run out has occurred.
7	When a 1, a send tally run out has occurred.
6	When a 1, the other system CMA detected a parity error on a byte sent to it. (status reported at end of send operation)
5	When a 1, the data transmission process was stopped by the receiving system turning its receive mode off.
4	When a 1, a data byte containing a parity error was received from the IOM. (status reported at end of send operation)
3	When a 1, a PCW containing a parity error was received from the IOM. (This PCW will not be executed.)
2	When a 1, the other system did not respond within the 250 (nom.) millisecond interval after send mode was set with a receive mode on indication or after a Data Available strobe with a Data Received strobe. (Resets send mode and causes status store)

3.5 STATUS WORDS (continued)

The functions of the receive status word bits are as follows:

Bit	Function
17-9	(same as for send status word)
8	When a 1, a pre tally run out occurred on the last byte stored indirect by the CMA.
7	When a 1, a receive tally run out has occurred.
6	When a 1, a parity error was detected on a data byte received from the other system. This will not be reported until the data transfer operation is completed.
5	When a 1, indicates that the other system send mode is on. When a 0, indicates that the other system send mode is off.
4	When a 1, indicates that a data byte transferred from the CMA to the IOM was received by the IOM with a parity error. This status is not reported until the data transfer operation is terminated.

3.6 SYSTEM MONITORING

One of the primary functions of the CMA is that of monitoring the operational status of the system in which it is installed. This will be accomplished by a hardware timer in the CMA which must be periodically reset by the 355 program. When the timer runs out (not reset in time), is disabled by the program, or the system loses power, a CMA-generated System Confidence signal will be turned off to indicate this condition to the other system in a dual configuration and to the communication line switch.

In order to turn the System Confidence signal on, the 355 program must issue a PCW to enable the "dead-man" timer. This will cause the CMA to turn the signal on and start a one second (nominal) timer. As long as the timer is enabled and does not run out, the System Confidence signal will remain on. The timer must be reset within one second by a PCW from the 355 program and within every one second time period thereafter.

In addition to the System Confidence signal, the CMA will provide a Switch Control signal to the communication line switch and to the other system in a dual configuration. This signal will be under control of the 355 program and will be used to indicate permission to connect the system to the communication lines.

4.0 INTERFACE REQUIREMENTS

4.1 IOM BUS

The CMA will interface with the DATANET 355 IOM via the IOM Bus as detailed in the 355 Computer EPS-1. The CMA will operate as a dynamic channel in the indirect mode.

4.2 OTHER SYSTEM CMA

The two CMA's in a dual system configuration will be interconnected by means of a multiconductor cable connected to a free-edge connector on each CMA. Cable lengths up to 50 feet should be provided for in the design.

Signals which must be communicated from each of the systems to the other system include the following:

- o Data plus odd parity (10 lines)
- o Data Available strobe
- o Data Received signal
- o Response strobe
- o Send mode indication
- o Receive mode indication
- o System Confidence signal
- o Switch Control signal

Since the CMA is to be capable of two-way-simultaneous operation, the above signals must be provided in each direction of transmission. If other signals are required because of the implementation, they must be provided in both directions of transmission so that the interface remains completely symmetric since the primary/secondary relationship of the two systems is variable.

4.3 COMMUNICATION LINE SWITCH

The communication line switch will be connected to the CMA by means of a multiconductor cable terminating at a free-edge connector on the CMA. Cable lengths up to 50 feet should be provided for in the design.

The following interface signals are required:

- From CMA to switch: System Confidence signal
  Switch Control signal
- From switch to CMA: Switch position (system A or B)
  Switch mode (manual or automatic)

Actuation of the communication line switch while in the automatic mode will be governed in part by the two signals generated by the CMA, and each system in a dual configuration is notified of the switch state.

5.0 GENERAL DESIGN REQUIREMENTS

The Computer Monitor Adapter channel shall conform to the requirements of Engineering Product Specification, General Design Requirements for the 655 and 355 Systems, Drawing Number 43A177851.

6.0 RELIABILITY AND MAINTAINABILITY

6.1 MEAN TIME BEFORE FAILURE (MTBF)

The MTBF goal for the CMA, as specified in the Message Switching specification, is:

$$MTBF - 40 \times 10^3 \text{ hours}$$

This figure must be met in order to achieve the 0.99995 availability goal for a dual system message switching configuration. Projected calculations based on the hardware implementation and component complement of the CMA, should meet the above requirements.

6.2 BOARD TESTER COMPATIBILITY

The CMA channel shall be designed such that the MQX Board Tester may be used to isolate faults. The board shall meet the criteria as defined in the MQX Board Tester EPS-1, drawing number 43A177854.

6.3 MAINTENANCE FEATURES

The design of the CMA will provide access to all control registers from the test and diagnostic program by means of PCW's and status words. In addition, two features intended to enhance the test and diagnostic programs effectiveness will be included. These features are wraparound of all external interface lines under program control and a special PCW command for testing the parity checking logic while in the wraparound mode.

When the wraparound mode is set by the program (see Section 3.2.1) the external interface lines will be wrapped back on one another as follows:

Interface to other system CMA

Since this interface is completely symmetrical (for each signal sent to the other system a corresponding signal is received from the other system) each send interface lead will be wrapped back on the corresponding receive lead. See Section 4.2.

Interface to communication line switch

System Confidence lead will be wrapped back on Switch Position lead. Switch Control lead will be wrapped back on Switch Mode lead.

While in the wraparound mode, it will be possible to check the operation of the parity checking logic (pertaining to data received from the other system CMA) by inverting the parity bit in the send data byte under program control (PCW bit 29). This feature will be disabled when the wraparound mode is not set.

ENGINEERING PRODUCT SPECIFICATION, PART 1
COMPUTER MONITOR ADAPTER

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